REMARKS

This amendment is responsive to the non-final Office Action dated April 22, 2004. Claims 1 - 4 are pending in this application. Claims 1, 2 and 4 have been rejected and claim 3 has been objected to. The following remarks follow the order of the outstanding Office Action beginning at page 2 thereof.

Drawings

The drawings has been amended and corrected drawings are submitted with this amendment.

Claim Rejections - 35 USC § 103

Claims 1 and 4

Applicant respectfully traverses the rejection of claims 1 and 4 as being unpatentable over Eino '025 in view of Takayama '961. Reexamination is respectfully requested in light of the following discussion.

This is a rejection of claim 1 under 35 USC § 103, which requires that the claim be considered as a whole with all of its elements. Claim 1 states that this is an electronic endoscope to whose front end an imaging device is set. This would correspond to Eino's element (12). Eino, like Applicant, has a processor unit connected to the CCD (12) and is directed to the problem of

providing a control circuit for generating a delay signal corresponding to a length of the electronic endoscope. Eino solves this problem by providing a signal delay line assembly in combination with a multiplexer (78). Eino provides a single multiplexer (78) with corresponding control lines P_1 - P_3 and P_G. Eino discloses that these control lines may be addressed in a manner of connecting pins, but also may be set by means provided on the video processor (24) (see column 8, lines 42 - 46). Eino, however, fails to provide a first reference-delay-time generation circuit for generating a signal having a rough reference delay time, and a second short-delay-time generation circuit for generating a signal having a delay time shorter than a reference delay time of the reference-delay-time generation circuit.

The operation of Applicant's reference-delay-time generation circuit and short-delay-time generation circuit are best understood by reference to Applicant's drawings. The microcomputer (18) provides two bits (four selections) to a multiplexer (25) which selects one of four clock signals S_A - S_D, which are derived from the reference-delay-time generation circuit. The computer, therefore, provides one of four reference-delay-time generation signals to the short-delay-time generation circuit. The short-delay-time generation circuit is shown in Figure 3. In Figure 3, there are a plurality of CMOS short-delay-time generation circuits (26a)-(26f). Each one of these short-delay-time generation circuits provides a delay in the nanosecond

order (see Applicant's specification, page 7, lines 12 - 13). The time for a signal to pass through a device such as (26a) is extremely short and measured in nanoseconds. The relationship of this time is best envisioned in reference to Figure 4 which depicts a short-time delay t_S relative to the base clock and drive clock as well as signals S_A - S_D.

When Applicant's two multiplexer signals are considered together as shown in Figures 2 and 3, it can be seen that there number of possible delays can be equal to the number from the reference- delay-time generation circuit (4) times the number of short delay time generation signals (6) or 4 x 6 = 24. In this manner, Applicant utilizes computer (18) to control both multiplexers (25) and (27) in order to achieve a high number of controlled time delays. Claim 1, however, does not require a multiplexer (this is in claim 3 which is allowable). Claim 1 does require the combination of the two delay-time generation circuits to control a delay signal.

Eino '025

Eino '025, unlike Applicant, has a single multiplexer and single delay scheme which is delay lines (80). Applicant in the description of prior art, beginning at page 1 and continuing to Applicant's page 2, describes a similar system. Eino discloses that if the maximum time delay is in the order of 200 nanoseconds, each sample and hold may only be 10 nanoseconds. This would

corresponds to taps T_1 to T_{20} in the delay line device (80) shown in Figure 6 of Eino.

The Examiner correctly observes that Eino does not disclose a short-delay-time generation circuit for generating a signal having a delay time shorter than a reference delay time of the reference-delay-time generation circuit. Applicant notes that Eino simply does not disclose more than one delay time generation circuit, be it short or a reference and does not disclose generating a delay signal in cooperation with a reference-delay-time and a short-delay-time generation circuit.

Takayama '961

Applicant respectfully traverses the rejection based upon Takayama '961 and requests reconsideration of this rejection. Takayama '961 does not suggest any modification to Eino '025 for the reason that Takayama does not utilize an endoscope having a CCD device at its tip, which requires compensation in a processing unit to adjust for different endoscope lengths. As shown in Figure 1 of '961, Takayama has an objective lens (17), optical fibers (11) and (12), and an endoscope portion (13). All of the Takayama control circuitry is directed to controlling the camera and electronics which are attached to the endoscope (2) . There is no change in length of endoscope portion (13). Instead, '961 is a simple photographic method having time controls for the photography system. The various delays used in '961 are for

control of the photography sequence, not for control of timing in order to adjust for endoscope length which provides delay signals which are required when endoscope length varies.

The control circuits of Takayama '961 are wholly inappropriate for any combination with '025 because the timing in '961 is dependent upon RC timing circuits, not upon fast acting devices which Applicant utilizes in the claimed short-delay-time generation circuit. All '961 teaches is five separate delay circuits (34), (52), (54), (56) and (36), each of which have a different function in the sequence control of the camera device attached to the endoscope. The first delay circuit (34) is related to a shutter drive circuit (35) which responds to a delayed output of the first delayed circuit. The second delay circuit (52) receives an output from a sequence control circuit (51) and becomes operative after a mirror shutter (20) has been opened). This in turn relates to exposure control. Description of the third, fourth and fifth delay circuits shows that each of these in turn is related to functions of the camera device, and has absolutely nothing to do with timing related to an imaging device which has a delay problem because of endoscope length. In summary, '961 shows delays used in a camera control circuit, which are wholly independent of and unrelated to any length of an electronic endoscope. As stated in Applicant's claim 1, the control circuit for generating a delay signal must correspond to a length of the electronic endoscope in cooperation with these timed

generation delay circuits. There simply is no such control circuit found in the combination of the two references because '961 does not suggest a delay-time generation circuit which would be responsive to imaging device for generating a delay signal corresponding to length (Applicant's claim 1). The reason this suggestion is lacking is that '961 does not include an imaging device and is in fact a well known early prior art device using optical fiber technology and a simple front end lens.

Claim 2

Claim 2 has been rejected as being unpatentable over Eino '025 and Takayama '961 as applied to claim 1 and further in view of Inaba '961. This rejection is respectfully traversed, first on the grounds stated with respect to claim 1.

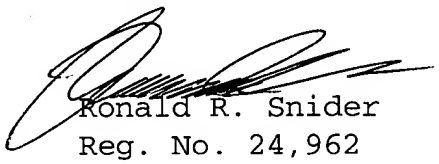
Inaba '961, like Takayama '961, does not relate to an electronic endoscope to whose front end an imaging device is set and generating a delay signal corresponding to length. Inaba has no length problem because of the failure to include the imaging device at the tip and, hence, simply cannot suggest the use of a gate device for any purpose, much less as claimed by Applicant. Inaba teaches in column 4, lines 45 - 50 that a multi-channel analyzer may have two inputs, one of which is from a gate delay generator (21). Applicant respectfully traverses the Examiner's observation that Inaba suggests gates can be used to provide short-delay-time signals. Instead, Applicant submits that column

4, lines 45 - 55 states that the gate signal obtained from the pulse signal A is greatly delayed by varying the delay time and can output this gate signal to the MCA (23). The portion relied upon neither discloses a plurality of gates, nor does it disclose a relationship between short and long time periods as claimed. Claim 2 claims the short-delay-time relative to the rough reference delay time. Inaba '961, like Takayama '961, simply fails to teach or suggest the use of any delay combination as set forth in claim 1. Still further, the specific use of the plurality of gate delay devices is simply not suggested in '961 which shows only a single gate delay generator (21) which is fed to the multi-channel analyzer.

The Examiner argues that it would be obvious to one of ordinary skill in the art to combine Eino, Takayama and Inaba for delaying the signals to obtain more accurate image of the captured endoscope scene. Applicant respectfully submits that these three references are completely non-analogous to each other because only one even relates to an electronic endoscope whose front end has an imaging device (CCD) and a processor to apply predetermined signal processing to a video signal from the imaging device. There is no evidence within the references cited which would show that a camera lens control system combined with a scinallation probe control system would have any effect whatsoever on image control for a CCD based device (Applicant claims an electronic endoscope).

In view of the foregoing, it is respectfully submitted that the application is now in condition for allowance, and early action in accordance thereof is requested. In the event there is any reason why the application cannot be allowed in this current condition, it is respectfully requested that the Examiner contact the undersigned at the number listed below to resolve any problems by Interview or Examiner's Amendment.

Respectfully submitted,



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